

Curriculum Vitae

William R. Mark

(updated June 13, 2009)

Work Contact: Intel Corporation; Building SC-12, MS 303
3600 Juliette Ln.
Santa Clara, CA 95054-1540
Phone: +1.408.623.8463; email: william dot r dot mark at intel dot com

Personal Contact: 269 Pettis Ave. Mountain View, CA 94041
Phone: +1.650.964.7264; email: billmark at billmark dot com

EMPLOYMENT HISTORY

Intel Corporation (Jan. 2008 – present)

Group Leader, Advanced Graphics Research, Intel Labs

Lead exploratory research and prototype system building for future real-time 3D graphics systems.

University of Texas at Austin (Jan. 2003 – Dec. 2007)

Assistant Professor, Department of Computer Sciences.

Investigating algorithms, hardware architectures, and programming environments for future real-time 3D graphics systems and general-purpose single-chip parallel computers.

NVIDIA Corporation (Oct. 2001 – Oct. 2002)

Lead architect / system designer for the Cg system (Cg is the first publicly-available commercial programming language and compiler for programmable graphics hardware). Worked with company management to define the product and development goals, and to build a ten-person system design and development team. Lead the design of the Cg language and wrote most of the language specification. Developed the first backend module for the Cg compiler.

Stanford University (May 1999 – Sept. 2001)

Postdoctoral Research Associate in Stanford Computer Graphics Lab (working with Pat Hanrahan). Co-lead a project to develop a high-level language for programming real-time graphics hardware, and co-advised students working on a project to demonstrate the potential to efficiently map ray tracing computations to mainstream graphics hardware. These efforts led to ongoing research into the use of programmable graphics hardware for scientific computation and for interactive volume rendering. In cooperation with Pat Hanrahan, coordinated/advised three doctoral students, one masters student, three undergraduates, and one staff programmer. Wrote short research proposals for funding from ATI, SONY, SGI, and 3dfx. Co-taught (with Marc Olano) a class on real-time programmable shading.

University of North Carolina, Chapel Hill (1992-1999)

Research Assistant in Computer Graphics Laboratory.

Investigated the use of image-based techniques to accelerate real-time 3D graphics.

Developed (with several other students) a client-server software system that allowed real-time graphics applications to incorporate high-fidelity haptics (force display).

Silicon Graphics Computer Systems (Summer 1995)

Software developer on the team designing the Nintendo-64 game console's hardware and system software. Wrote software tools and code examples that were provided to game developers.

Rice University (Summer 1991 & 1992)

Research Assistant in Rice Quantum Institute (1992): Continued physics research from senior thesis.
Research Assistant in Bonner Nuclear Research Lab (1991): Wrote computer code to model part of a detector for the proposed Superconducting Super Collider.

EDUCATION

University of North Carolina at Chapel Hill

Ph.D., Computer Science, May 1999.

Dissertation: *Post-Rendering 3D Image Warping: Visibility, Reconstruction, and Performance for Depth-Image Warping.*

Rice University

B.A. *cum laude*, Physics, May 1992.

Senior Thesis: *Lifetime measurement of an excited vibrational level of the 1B_2 excited state of ozone by a modification of the technique of stimulated emission pumping.*

REFEREED PUBLICATIONS

Data Parallel Rasterization of Micropolygons with Defocus and Motion Blur,
Kayvon Fatahalian, Edward Luong, Solomon Boulos, Kurt Akeley, William R. Mark, Pat Hanrahan.
High Performance Graphics 2009, August 2009 (to appear).

Soft Irregular Shadow Mapping: Fast, High-Quality, and Robust Soft Shadows
Gregory Johnson, Allen Hux, Chris Burns, Warren Hunt, Stephen Junkins, William R. Mark
2009 Symposium on Interactive 3D Graphics, Feb, 2009.

Venkatraman Govindaraju, Karthikeyan Sankaralingam, Mary Vernon, Peter Djeu, William R. Mark. "A Multi-core Architecture for Real-time Ray-tracing," 41st Annual IEEE/ACM Intl. Symp. on Microarchitecture (MICRO 2008), Nov. 2008.

Warren Hunt and William R. Mark. "Ray-specialized acceleration structures for Ray Tracing," 2008 IEEE/EG Symposium on Interactive Ray Tracing, August 2008.

Warren Hunt and William R. Mark. "Adaptive acceleration structures in perspective space," 2008 IEEE/EG Symposium on Interactive Ray Tracing, August 2008.

Ryan Overbeck, Ravi Ramamoorthi, and William R. Mark. "Large Packets for Real-time Whitted Ray Tracing," 2008 IEEE/EG Symposium on Interactive Ray Tracing 2008.

William R. Mark. "Future Graphics Architectures," ACM Queue, March/April 2008. (Invited paper for special issue on graphics architectures)

Warren Hunt, William R. Mark, and Donald Fussell. "Fast and Lazy Build of Acceleration Structures from Scene Hierarchies", 2007 IEEE Symposium on Interactive Ray Tracing, Sept 2007.

Paul Navratil, Donald Fussell, Calvin Lin, and William R. Mark. "Dynamic Ray Scheduling for Improved System Performance," 2007 IEEE Symposium on Interactive Ray Tracing, Sept 2007.

Ryan Overbeck, Ravi Ramamoorthi, and William R. Mark. "A Real-time Beam Tracer with Application to Exact Soft Shadows," 2007 Eurographics Symposium on Rendering, June 2007.

Ingo Wald, William R. Mark, Johannes Gunther, Solomon Boulos, Thiago Ize, Warren Hunt, Steven G. Parker, and Peter Shirley. "State of the Art in Ray Tracing Animated Scenes," Eurographics 2007 State of the Art Report. (Note: This article is a review article; an extended abstract was peer-reviewed but the full paper was not).

Peter Djeu, Warren Hunt, Rui Wang, Ikrima Elhassan, Gordon Stoll, William R. Mark. "Razor: An architecture for dynamic multiresolution ray tracing," (conditionally accepted April 3, 2007 to ACM Transactions on Graphics, not yet fully revised).

Warren Hunt, William R. Mark, Gordon Stoll. "Fast kd-tree Construction with an Adaptive Error-Bounded Heuristic," 2006 IEEE Symposium on Interactive Ray Tracing, Sept 2006.

Gregory S. Johnson, Juhyun Lee, Christopher A. Burns, William R. Mark. "The Irregular Z-Buffer: Hardware Acceleration for Irregular Data Structures," ACM Transactions on Graphics, Oct. 2005.

Karthikeyan Sankaralingam, Stephen W. Keckler, William R. Mark, Doug Burger. "Universal Mechanisms for Data Parallel Architectures," 36th Annual International Symposium on Microarchitecture (MICRO-36), December, 2003.

William R. Mark, R. Steven Glanville, Kurt Akeley, Mark J. Kilgard. "Cg: A System for Programming Graphics Hardware in a C-like Language," ACM Transactions on Graphics, Vol 22, #3, July 2003 (SIGGRAPH 2003).

Tim Purcell, Ian Buck, William R. Mark, and Pat Hanrahan, "Ray Tracing on Programmable Graphics Hardware." SIGGRAPH 2002.

Kekoa Proudfoot, William R. Mark, Svetoslav Tzvetkov and Pat Hanrahan, "A Real-Time Procedural Shading System for Programmable Graphics Hardware." SIGGRAPH 2001.

William R. Mark and Kekoa Proudfoot, "Compiling to a VLIW Fragment Pipeline." SIGGRAPH/Eurographics Workshop on Graphics Hardware 2001.

William R. Mark and Kekoa Proudfoot, "The F-Buffer: A Rasterization-Order FIFO Buffer for Multi-Pass Rendering." SIGGRAPH/Eurographics Workshop on Graphics Hardware 2001.

William R. Mark and Gary Bishop, "Memory Access Patterns of Occlusion-Compatible 3D Image Warping." SIGGRAPH/Eurographics Workshop on Graphics Hardware 1997.

William R. Mark, Leonard McMillan, and Gary Bishop, "Post-Rendering 3D Warping." 1997 Symposium on Interactive 3D Graphics.

William R. Mark, Scott Randolph, Mark Finch, James Van Verth, and Russell M. Taylor II, "Adding Force Feedback to Graphics Systems: Issues and Solutions." SIGGRAPH 1996.

BOOK CHAPTER

“Real-time programmable shading” in “Texturing and Modeling: A Procedural Approach,” David S. Ebert *et al.*, third edition, Morgan-Kaufmann, 2003.

TECHNICAL REPORTS

Gordon Stoll, William R. Mark, Peter Djeu, Rui Wang, and Ikrima Elhassan, “Razor: An architecture for dynamic multiresolution ray tracing”, University of Texas at Austin, Department of Computer Sciences Technical Report TR-06-21, April 26, 2006.

William R. Mark and Donald Fussell, “Real-Time Rendering Systems in 2010.” University of Texas at Austin Computer Sciences Technical Report TR-05-18, May 2, 2005.

Gregory S. Johnson, William R. Mark and Christopher A. Burns, “The Irregular Z-Buffer.” University of Texas at Austin Computer Sciences TR-04-09, April 15, 2004.

William R. Mark, “Post-Rendering 3D Image Warping: Visibility, Reconstruction, and Performance for Depth-Image Warping.” (Ph.D. Thesis), UNC Computer Science TR #99-022, April 1999

William R. Mark and Gary Bishop, “Efficient Reconstruction Techniques for Post-Rendering 3D Image Warping” UNC-CH Computer Science TR #98-011, January 21, 1998.

William R. Mark, Gary Bishop, and Leonard McMillan, “Post-Rendering Image Warping for Latency Compensation.” UNC-CH Computer Science TR #96-020, January 10, 1996.

William R. Mark, Scott C. Randolph, Mark Finch, and James M. Van Verth, “UNC-CH Force Feedback Library, Revision C.” UNC-CH Computer Science TR #96-012, January 30, 1996.

SELECTED PRESENTATIONS

Panelist, Jon Peddie Research panel on “Ray Tracing and Rasterization”, August 13, 2008.

Invited panel presentation for “GPUs vs. Multicore CPUs: On a converging course or fundamentally different?”, Graphics Hardware 2008, June 20, 2008.

Invited panel presentation on the future of graphics hardware and the graphics hardware conference (panel title “Whiter graphics hardware, and Graphics Hardware”), Graphics Hardware 2007, August 4, 2007.

“State of the art in interactive ray tracing”, SIGGRAPH 2006 course, July 30, 2006, course presenter.

"Real-time rendering in 2010 and beyond", University of North Carolina at Chapel Hill, Nov 11, 2005

Invited panel presentation for "Innovative Application Areas in 201X", Intel many-core conference, Portland, OR, Dec 8, 2005.

“Real-Time Graphics in 2010”,

University of Washington, August 16, 2005
Microsoft Research, August 17, 2005

“Introduction to Real-Time Ray Tracing” SIGGRAPH 2005 Course, August 3, 2005, course presenter.

“3D Graphics Hardware: Evolution Now, Revolution Later,” William R. Mark, invited panel presentation for Graphics Hardware 2005 panel “3D Graphics Hardware: Revolution or Evolution?”, July 31, 2005.

“Real-time graphics architecture,” William R. Mark and Henry Moreton, MICRO 2004 Tutorial, Dec. 4, 2004.

“Future Visualization Platform”, Invited panel presentation at Visualization 2004 conference, Oct. 14, 2004.

“CPUs vs. GPUs”, Invited presentation at GP² workshop panel on “GPUs and CPUs: The Uneasy Alliance?”, August 8, 2004.

SIGGRAPH 2000, 2001, 2002, and 2003: Course presentations on programming languages and compilers for graphics hardware.

“Cg: A System for Programming Graphics Hardware in a C-like Language,” and “3D Graphics (Rendering) Overview,” Streaming Systems Workshop, MIT Endicott House, August 22-23, 2003.

“Cg: A System for Programming Graphics Hardware in a C-like Language,” and “The Next Major Change in Real-Time Graphics: The Transition to General-Purpose Parallel Hardware”, Microsoft Research, July 2, 2003.

“The Co-Evolution of Graphics Architectures, Algorithms, and Programming Interfaces,” Intel Microprocessor Research Lab, June 6, 2003.

Invited keynote speaker, Graphics Hardware 2002 conference, Sept 1, 2002.
“Programmable graphics hardware: Beyond real-time movie rendering”

Game Developer’s Conference, “Shading Languages for Graphics Hardware”, March 23, 2001.

Workshop on Image Synthesis and Interactive 3D Graphics, Dagstuhl, Germany, “Real-Time Programmable Shading”, June 19, 2000.

Other talks on programming systems for graphics hardware:

Caltech, Oct. 21, 2002.

University of Washington, July 26, 2001.

Pixar, March 27, 2001.

University of Utah, March 9, 2001.

Microsoft Research, January 15, 2001.

Max-Planck Institute (Informatik), June 15, 2000.

NVIDIA hardware architecture group, June 7, 2000.

University of North Carolina, May 18, 2000 and Oct 14, 2002.

PROGRAM COMMITTEES

General co-chair, 2008 IEEE Symposium on Interactive Ray Tracing, August 9-10, 2008.

Papers co-chair, 2006 IEEE Symposium on Interactive Ray Tracing, Sept 18-20, 2006.

Papers co-chair, SIGGRAPH/Eurographics Graphics Hardware conference, 2003.

Program committee, Eurographics Symposium on Rendering, 2008-2009.

Program committee, Symposium on Interactive 3D Graphics and Games, 2008.

Program committee, ACM/Eurographics High Performance Graphics, 2009.

Program committee, SIGGRAPH/Eurographics Graphics Hardware conference, 2001-2008.

Program committee, IEEE Symposium on Interactive Ray Tracing, 2007.

COURSES TAUGHT

Computer Architecture (undergraduate), Spring 2007 (UT), Spring 2005 (UT) , Spring 2004 (UT) , Spring 1994 (UNC).

Computer Graphics (graduate and honors undergraduate), Fall 2004, Fall 2005 , Fall 2007 (UT).

Fine-grained parallelism, Spring 2006, Graduate Seminar, UT Austin

High-Performance Ray Tracing for Dynamic Scenes (w/ Don Fussell), Fall 2003, Grad. Seminar (UT)

Economics of Technology (with Don Fussell), Fall 2003, Graduate Seminar, UT Austin

Real-Time Graphics Architectures, Algorithms, and Programming Systems, Spring 2003, UT Austin.
Graduate seminar covering topics relevant to future real-time 3D graphics systems and algorithms.

Real-time programmable shading (with Marc Olano), Spring 2000, Stanford University.
A research-topics course for graduate students and advanced undergraduates.

VISITING RESEARCH and CONSULTING

Neoptica, occasional consultant, 2006 and 2007.

Intel Corporation, Visiting Researcher, mid-May to mid-June 2005, and May to Nov, 2006.

NVIDIA, Consultant, Spring and Summer 2001.

RESEARCH FUNDING

While at UT Austin (January 2003-December 2007)

NSF CAREER award, \$400,000, February 2006,

“CAREER: A systems approach to real-time graphics on single-chip highly-programmable hardware”

Lead PI on over \$570,000 (already received) in industry gift funds and graduate student fellowship funding from Microsoft, Intel, NVIDIA, and ATI/AMD.

Lead PI on over \$100,000 (already received) in equipment donations from Intel, NVIDIA, and ATI.

REVIEW PANELS

NSF proposal review panelist, Nov 2006.

External reviewer for DOE / LANL internally funded project on using GPUs and FPGAs for high performance computing, July 27, 2005.

HONORS

NSF CAREER award, Feb. 2006.

Game Developer Magazine 2002 “Front Line Award”, recognizing Cg.